REMARKS

Reconsideration of this application is respectfully requested.

THE PRESENT INVENTION

According to the present invention as recited in claim 1, a circuit for generating dot clock pulses for driving a light-emitting element employed in an optical-writing section of an image-forming apparatus is provided which comprises:

- (i) a digital-delay dot clock adjusting section to adjust timings of rising-edges or falling-edges of dot clock pulses generated by changing a selection for a plurality of delayed-clock pulses, which are generated by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times; and
- (ii) a controlling section to control a selecting operation for the plurality of delayed clock pulses, performed in the digital-delay dot clock adjusting section, so as to compensate for unevenness of scanning-light amount caused by an optical element employed in the optical-writing section.

With this clock generating circuit, since the unevenness of scanning-light amount caused by the optical element employed in

the optical-writing section can be automatically compensated for by controlling a selecting operation for the plurality of delayed clock pulses, it becomes possible to achieve an image-forming apparatus employing a polygon mirror in its optical writing system in which the negative influence of unevenness of the scanning-light amount (the shading effect) is reduced so that image quality can be improved.

Similarly, according to the present invention as recited in independent claim 2, a circuit for generating dot clock pulses is provided which comprises a delay-chain section to generate a plurality of delayed-clock pulses, a delayed-clock switching section to generate a select signal for selecting a specific delayed-clock pulse for compensating for unevenness of scanning light amount caused by an optical element employed in an optical-writing section, and a selector for selecting the specific delayed-clock pulse. Again, with this clock generating circuit, since the unevenness of scanning-light amount caused by the optical element employed in the optical-writing section can be automatically compensated for by controlling a selecting operation for the plurality of delayed clock pulses, it becomes possible to achieve an image-forming apparatus employing a polygon mirror in its optical writing system in which the

negative influence of unevenness of the scanning-light amount (the shading effect) is reduced so that image quality can be improved.

Still further, it is respectfully pointed out that independent claims 7 and 8 recite image-forming apparatuses employing the clock generating circuits of claims 1 and 2, respectively. And it is also respectfully pointed out that claims 3-6 and 9-12 depend from claims 2 and 8, respectively, and recite further features of the clock generating circuits of claims 2 and 8, respectively.

THE PRIOR ART REJECTION

Claims 1-12 were rejected under 35 USC 102 as being anticipated by JP 2000-198235 ("Takagi et al"). This rejection, however, is respectfully traversed.

On pages 2-4 of the Office Action, the Examiner asserts that the clock pulse generating circuit disclosed in Takagi et al is totally equivalent to the clock pulse generating circuit of the claimed present invention.

It is respectfully submitted, however, that the clock pulse generating circuit of Takagi et al has no function for compensating for unevenness of scanning-light amount caused by an

optical element employed in an optical-writing section, as according to the claimed present invention.

Instead, Takagi et al (which is owned by the same corporate entity as the claimed present invention) merely discloses a clock pulse generating circuit which comprises a delay section (410) for generating a plurality of delay clocks of different phase by delaying a reference clock, sections 420, 430 for detecting shift of images formed on an image carrier by an exposing means, a delay clock switching control section 440 for determining the phase correction amount of each color from the shift of the images and for then determining which phase of the delay clock should be selected for each color, and a section 450 for selecting a delay clock from the delay section for each color and supplying it, as a dot clock, to the exposing means. That is, Takagi et al merely discloses a clock pulse generating circuit whose purpose is to eliminate fluctuations of the lengths of the scanning lines formed on image-bearing members by plural exposure means, so as to prevent the reproduced full-color image from having color deviation.

And it is respectfully submitted that the disclosure in Takagi et al provides absolutely no teaching or suggestion to one of ordinary skill in the art to achieve the advantageous

structure and effects of the clock generating circuit and image forming apparatus of the claimed present invention which compensate for unevenness of scanning-light amount caused by an optical element employed in the optical-writing section. Indeed, Takagi et al teaches nothing at all relating to a dot clock pulse generating circuit having a function for compensating for unevenness of scanning-light amount caused by an optical element employed in an optical-writing section, as according to the claimed present invention.

In view of the foregoing, it is respectfully submitted that the present invention as recited in each of independent claims 1, 2, 7 and 8, as well as each of claims 3-6 and 9-12 respectively depending from claims 2 and 8, clearly patentably distinguishes over Takagi et al, taken singly or in combination with any of the other prior art references of record, under 35 USC 102 as well as under 35 USC 103.

Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,

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